Amendments to the Specification

Please replace Page 2, Lines 11-15 as follows:

On a logical level, the logical circuits are designed using simulation systems wherein a circuit design is expressed in a hardware description language (HDL). An example ~~for~~ of a hardware description language is Verilog as described by IEEE Standard 1364 and an example for a simulation system is NCVerilog available from Cadence, 2655 Scely Avenue, San ~~Jos~~ Jose, Calif. 95134.

Please replace Page 2, Lines 16-18 as follows:

Normally, when developing a circuit design, the majority of simulation work is done on a ~~"cycle level". Simulation~~ cycle level. Cycle level simulation comprises ~~basically~~ [[of]] a sampling process which acquires states of a circuit design.

Please replace Page 3, Lines 4-6 as follows:

Therefore, it is an object of the present invention to provide a method and system for circuit simulation that allows ~~to find~~ for the finding of faults easier in the design and to identify them earlier in the design cycle.

Please replace Page 3, Lines 7-12 as follows:

In one embodiment ~~according to the~~ of the present invention, a method for simulation of an electronic circuit is ~~provided, the~~ provided. The circuit being represented by a network of a plurality of logic ~~elements, the~~ elements. The circuit ~~comprising~~ comprises a first and second asynchronous clock ~~domains~~ domain, whereby jitter elements are additionally inserted at predetermined portions of [[the]] circuit

boundaries between the first and second asynchronous clock ~~domains, the~~ domains. The jitter elements being represented as logic elements, the values of which are randomly set.

Please replace Page 4, Lines 4-9 as follows:

A further embodiment of the present invention provides for a simulation system for simulating an electronic ~~circuit, the~~ circuit. The circuit being representable by a network of logical ~~elements, the~~ elements. The circuit ~~comprising~~ comprises a first and second asynchronous clock ~~domains~~ domain, wherein jitter elements are additionally insertable at predetermined portions of circuit boundaries between the first and second asynchronous clock ~~domains, the~~ domains. The jitter elements being representable as logical elements, the values of which are randomly set.

Please replace Page 4, Lines 10-11 as follows:

Preferably, the simulation may be carried out on [[a]] cycle level ~~of a~~ description of the electronic circuit.

Please replace Page 5, Lines 7-10 as follows:

One advantage of the invention is that faults in the design can be identified at a higher level of the design, resulting in quicker simulation times. Thus, simulations according to the invention will provide indications of failures at [[the]] cycle level rather than on [[a]] gate level.

Please replace Page 5, Lines 12-14 as follows:

A further advantage of the present invention is that it requires less memory, when implemented in [[a]] computer software, than methods ~~need~~ used for gate-level simulations.

Please replace Page 6, Line 19 through Page 7, Line 2 as follows:

FIG. 1 illustrates a section of a circuit diagram having two portions with two clock domains designated D1 and D2, respectively. In FIG. 1 the different clock domains are separated by dashed lines. FIG. 1 illustrates state of the art counter measures to reduce the probability of ~~meter stability~~ metastability in a logical circuit due to asynchronous clock domains.

Please replace Page 7, Lines 15-16 as follows

Jitter elements typically are inserted at any points where ~~data are~~ data is handed over different clock domains D1, D2.